Bi-weekly Status Report 6
Senior Design, December 2020, Team 14

Introduction of Real-World Signals and Systems into ECpE DSP Laboratory Curriculum

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Progress Summary:

In the past two weeks, we received the new CyDAQ boards and stencils, assembled them, and verified their performance will meet or exceed our requirements. We brought the SPI bus up to 50MHz and verified correct DAC behavior. We performed a full system test to ensure that the lab PC front-end, FPGA firmware, and redesigned hardware would operate together as intended. We also made significant progress on lab development, including software support for the DAD, full design and validation of the controls 2 lab, and partial implementation into CyDAQ. After validating the performance of CyDAQ and its compatibility with the DAD, we demonstrated its new features to ECpE faculty Julie Dickerson and Andrew Bolstad, in preparation for its integration into EE224 and EE324 labs.

Individual Contributions by Team Member:

- **Brady Anderson (Biweekly: 18; Cumulative: 162)**
    - Characterized SPI DAC maximum generation rate
        - Profiled and optimized DAC ISR code
    - Completed full system test with front-end software and new hardware
        - Increase SPI frequency to final 50 MHz
    - Demonstrated CyDAQ to DSP professors Julie Dickerson and Andrew Bolstad
- **Sam Burnett (Bi-weekly: 32, Cumulative: 210)**
    - Completed 2 full validation builds of Rev 2 PCB
    - Tested basic functionality of Rev 2 validation PCBs
    - Tested DAC functionality over SPI of validation build
    - Finalized PCB design of Rev 1 retrofit expansion PMOD and ordered boards
    - Generated BoM and ordered parts for Rev 1 retrofit expansion PMOD
    - Finished hardware section of team poster
    - Worked on final report and supporting documentation
- **Mitchell Hoppe (Weekly: 12; Cumulative: 134.0)**
    - Added more navigation functions for the user.
    - Presented CyDAQ to faculty group
- **Max Kiley (Bi-Weekly: 20; Cumulative: 146)**
    - Revised Lab 1 for EE 324.
    - Assemble the first prototype of a mechanical system.
    - Created another 3D printed damper for the mechanical system
    - Ordered another set of parts for lab 1's mechanical system
- **Emily LaGrant (Biweekly: 12; Cumulative: 139)**

    - Worked on final report
    - Worked on presentation poster
    - Worked on documentation for labs
- **Isaac Rex (Bi-Weekly: 14; Cumulative: 206)**
    - Finished mechanical build for controls lab 2
    - Finished Simulink model for system
    - Implemented prototype of controller using Arduino
    - Finished FPGA PL build of hardware and began porting code to Zynq
    - Presented CyDAQ developments and got feedback from Signal and System faculty
    - Finished DAD Laview implementation

Pending Issues:

- Live streaming of data to lab PCs may require some firmware design changes. UART RX process is polled but may also need to transmit periodically, necessitating a timeout or hybrid FreeRTOS approach
- UART cannot keep up with 1 MHz+ ADC sample rates, so some buffering will be necessary. Sliding R/W heads would maximize buffer utilization
- DAC generation is limited to < 8kHz by Xilinx SPI controller limitations. Implementing a custom SPI controller may improve performance

Plans:

- Isaac:
    - Finish Zynq port of PID controller
    - Polish controls 1 lab
    - Write controls 2 lab
- Emily:
    - Continue documentation for labs
    - Continue work on presentation, poster, and report
- Brady:
    - Integrade SPI ADC into main CyDAQ firmware
    - Investigate possible solutions for UART streaming mode
        - Probably using UART interrupts on command receive
- Sam:
    - Finish Testing the ADC on the validation boards
    - Build and test Rev 1 expansion PMODs
    - Finish all documentation and push everything to Git
- Max
    - Machine the mass to fit a larger bearing
    - Create a second revision of the mechanical system.
    - Update Solidworks drawings
- Mitch

- Add data format changes
- Add temp storage of parameters
- Fix bugs